IN THE CLAIMS:

1. (Previously Presented) A method of manufacturing a laterally diffused metal oxide semiconductor (LDMOS) device, comprising:

forming isolation structures and a gate structure;

forming an amorphous region in a semiconductor substrate between the isolation structures and adjacent the gate structure by implanting an amorphizing element in the semiconductor substrate; and

diffusing a channel dopant laterally in the amorphous region to form a first portion of a channel.

2. (Original) The method as recited in Claim 1 wherein implanting an amorphizing element includes implanting silicon.

3. (Original) The method as recited in Claim 2 wherein implanting silicon includes implanting silicon with an implant dose of at least about 1E15 atoms/cm^2.

4. (Withdrawn) The method as recited in Claim 1 wherein implanting an amorphizing element includes implanting germanium.

5. (Withdrawn) The method as recited in Claim 4 wherein implanting germanium includes implanting germanium with an implant dose of at least about 1E14 atoms/cm^2.

6. (Previously Presented) The method as recited in Claim 1 wherein diffusing a channel dopant laterally in the amorphous region includes diffusing a first P-type source/drain dopant to a depth of about 100 nm, and implanting an amorphizing element includes implanting an amorphizing element to a depth ranging from about 180 nm to about 200 nm.

7. (Previously Presented) The method as recited in Claim 1 wherein diffusing a channel dopant laterally in the amorphous region includes diffusing a channel dopant on a first side of the gate structure and further including diffusing a source/drain dopant laterally in the semiconductor substrate and on a second side of the gate structure.

8. (Previously Presented) The method as recited in Claim 1 wherein diffusing a channel dopant includes diffusing a channel dopant at a temperature above about 600°C that re-crystallizes the amorphous region.

9. (Previously Presented) The method as recited in Claim 1 wherein diffusing a channel dopant includes diffusing a channel dopant having a gaussian distribution within the amorphous region.

10. (Original) The method as recited in Claim 1 wherein forming an amorphous region includes forming an amorphous region using an energy ranging from about 50KeV to about 150 KeV.

11. (Previously Presented) A method of manufacturing an integrated circuit, comprising:

fabricating laterally diffused metal oxide semiconductor (LDMOS) transistors, including:

forming isolation structures and a gate structure;

forming an amorphous region in a semiconductor substrate between the isolation structures and adjacent the gate structure by implanting an amorphizing element in the semiconductor substrate; and

diffusing a channel dopant laterally in the amorphous region to form a first portion of a channel;

depositing interlevel dielectric layers over the LDMOS transistors; and

creating interconnect structures in the interlevel dielectric layers that interconnect the LDMOS transistors to form an operative integrated circuit.

12. (Original) The method as recited in Claim 11 wherein implanting an amorphizing element includes implanting silicon.

13. (Original) The method as recited in Claim 12 wherein implanting silicon includes implanting silicon with an implant dose of at least about 1E15 atoms/cm^2.

14. (Withdrawn) The method as recited in Claim 11 wherein implanting an amorphizing element includes implanting germanium.

15. (Withdrawn) The method as recited in Claim 14 wherein implanting germanium includes implanting germanium with an implant dose of at least about 1E14 atoms/cm^2.

16. (Previously Presented) The method as recited in Claim 11 wherein diffusing a channel dopant laterally in the amorphous region includes diffusing a first P-type dopant to a depth of about 100 nm, and implanting an amorphizing element includes implanting an amorphizing element to a depth ranging from about 180 nm to about 200 nm.

17. (Previously Presented) The method as recited in Claim 11 wherein diffusing a channel dopant laterally in the amorphous region includes diffusing a channel dopant on a first side of the gate structure and further including diffusing a source/drain dopant laterally in the semiconductor substrate and on a second side of the gate structure.

18. (Previously Presented) The method as recited in Claim 11 wherein diffusing a channel dopant includes diffusing a channel dopant at a temperature above about 600°C that re-crystallizes the amorphous region.

19. (Previously Presented) The method as recited in Claim 11 wherein diffusing a channel dopant includes diffusing a channel dopant having a gaussian distribution within the amorphous region.

20. (Original) The method as recited in Claim 11 wherein forming an amorphous region includes forming an amorphous region using an energy ranging from about 50KeV to about 150 KeV.